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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,554	07/01/2003	Wenge Yang	D982.D1	3624

22898 7590 06/28/2004

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EXAMINER	
HOGANS, DAVID L	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,554	YANG ET AL.	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *6-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *6-10* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the transmittal of a new application filed on July 1, 2003.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-5, drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 40.

   II. Claims 6-10, drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 640.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the subcombination requires the implanting of source and drain regions in the active region adjacent to the sidewall spacers. The subcombination has separate utility such as a transistor.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mikio Ishimaru on June 17, 2004, a provisional election was made with traverse to prosecute the invention of Group I, claims 1-5. Affirmation of this election must be made by applicant in replying to this Office action. Claims 6-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Status of Claims

Claims 1-5 are pending. Claims 6-10 are withdrawn. Claims 11-14 are cancelled.

Priority

7. This application appears to be a division of Application No. 09/974,917, filed October 10, 2001. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The

divisional application should set forth only that portion of the earlier disclosure which is germane to the invention as claimed in the divisional application.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of 6,392,310 to Matsunaga.

AAPA teaches forming a pair of multi-layer structures (210a and 210b) on an active region on the semiconductor substrate (102); forming sidewall spacers (230) around the pair of multi-layer structures; forming a dielectric liner layer (231) over the semiconductor substrate, including the pair of multi-layer structures, the sidewall spacers, the dielectric liner layer in contact with the active region; forming a dielectric layer (232) over the dielectric liner layer; forming a photoresist (238) over the dielectric layer; patterning and developing the photoresist to form a photoresist contact opening (234) therein; and removing the photoresist. (See Applicant's Figures 2-3 and pages 3-8 of Applicant's specification)

AAPA fails to teach forming a first tapered contact opening, using the photoresist contact opening, into the dielectric layer, forming the first tapered contact opening with a

bottom opening smaller than the photoresist contact opening; forming a second tapered contact opening, using the first tapered contact opening, into the dielectric liner layer, forming the second tapered contact opening with a bottom opening open to the active region for a smaller region than the active region with which the dielectric liner layer is in contact; and forming a conductive material in the first and second tapered contact openings to form a contact in contact with the active region, the dielectric liner laver, and the dielectric layer.

However, Matsunaga, in Figures 2-6 and columns 8-9 lines 01-48, teaches forming a first tapered contact opening (i.e. – formed in layer 5), using the photoresist contact opening, into the dielectric layer (5), forming the first tapered contact opening with a bottom opening smaller than the photoresist contact opening; forming a second tapered contact opening (i.e. – formed in layer 5B), using the first tapered contact opening, into the dielectric liner layer (5B), forming the second tapered contact opening with a bottom opening open to the active region for a smaller region than the active region with which the dielectric liner layer is in contact (noting Figure 6); and forming a conductive material (8A) in the first and second tapered contact openings to form a contact in contact with the active region, the dielectric liner layer, and the dielectric layer.

It would have been obvious to one of ordinary skill in the art to modify AAPA by incorporating forming a first tapered contact opening, using the photoresist contact

opening, into the dielectric layer, forming the first tapered contact opening with a bottom opening smaller than the photoresist contact opening; forming a second tapered contact opening, using the first tapered contact opening, into the dielectric liner layer, forming the second tapered contact opening with a bottom opening open to the active region for a smaller region than the active region with which the dielectric liner layer is in contact; and forming a conductive material in the first and second tapered contact openings to form a contact in contact with the active region, the dielectric liner laver, and the dielectric layer, as taught by Matsunaga, to reduce leakage current between a via and a gate electrode.

10. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of 6,392,310 to Matsunaga further in view of 6,407,002 to Lin et al.

Claims 2 and 3

Incorporating all arguments of Claim 1 and noting that AAPA and Matsunaga fail to explicitly teach forming a bottom anti-reflecting coating (BARC) on the dielectric layer before forming the photoresist over the dielectric layer to assist in patterning the photoresist, wherein the BARC has a tapered opening.

However, Lin et al., in Figure 3 and columns 5-8 lines 65-68, teaches forming a bottom anti-reflecting coating (330) on the dielectric layer (320) before forming the

photoresist (340) over the dielectric layer to assist in patterning the photoresist, wherein the BARC has a tapered opening.

It would have been obvious to one of ordinary skill in the art to modify AAPA and Matsunaga by incorporating forming a bottom anti-reflecting coating on the dielectric layer before forming the photoresist over the dielectric layer to assist in patterning the photoresist, wherein the BARC has a tapered opening, as taught by Lin et al., to provide a hard mask that can better control critical dimensions by minimizing standing wave effects.

11. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of 6,392,310 to Matsunaga further in view of 6,407,002 to Lin et al. further in view of 6,271,117 to Cherng.

Claim 4

Incorporating all arguments of Claim 1 and noting that AAPA, Matsunaga and Lin et al. fail to explicitly teach wherein forming a tapered contact opening uses an etching process.

However, Cherng, in Figures 1-4 and columns 3-5 lines 35-62, teaches wherein forming a tapered contact opening uses an etching process.

It would have been obvious to one of ordinary skill in the art to modify AAPA, Matsunaga and Lin et al. by incorporating wherein forming a tapered contact opening uses an etching process, as taught by Cherng, to form a tapered contact opening.

Claim 5

Incorporating all arguments of Claim 1 and noting that AAPA, Matsunaga and Lin et al. fail to explicitly teach wherein forming a conductive material includes: depositing the conductive metal over the dielectric layer and in the tapered contact opening; and planarizing the conductive metal flush with the dielectric layer.

However, Cherng, in Figures 1-4 and columns 3-5 lines 35-62, teaches wherein forming a conductive material includes: depositing the conductive metal over the dielectric layer and in the tapered contact opening; and planarizing the conductive metal flush with the dielectric layer.

It would have been obvious to one of ordinary skill in the art to modify AAPA, Matsunaga and Lin et al. by incorporating wherein forming a conductive material includes: depositing the conductive metal over the dielectric layer and in the tapered contact opening; and planarizing the conductive metal flush with the dielectric layer, as taught by Cherng, to reduce topography variations and increase chip packing density.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 4,902,377 to Berglund et al. teaches etching sloped via sidewalls in a dielectric to form a contact to an interconnect.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (571) 272-1691. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DH

JACK CHEN
PRIMARY EXAMINER